Printed	Pages	_	4
---------	-------	---	---

Roll No.

333356(33)

B. E. (Third Semester) Examination, April-May 2021

(New Scheme)

(IT Branch)

DIGITAL ELECTRONICS and LOGIC DESIGN

Time Allowed: Three hours

Maximum Marks: 80

Minimum Pass Marks: 28

Note: Part (a) from each question is compulsory carrying 2 marks. Attempt any two parts from (b), (c) and (d) of each question carrying 7 marks each.

Olynt sage Clean han Unit-I

1. (a) Compare BCD with Binary.

2

(b) Write down the steps to minimize Boolean expression and also discuss different theorem involve in it.

7

(c)	Minimize the following boolean function using	K
	Map:	31/2+31/2

(i)
$$F_1(A, B, C, D, E) = \sum m(0, 2, 5, 7, 9, 11, 13, 15, 16, 18, 21, 23, 25, 27, 29, 31)$$

(ii)
$$F_2(A, B, C, D) = \pi m (1, 5, 6, 12, 13, 14) + d(2, 4)$$

(d) Solve following Boolean function using Quine-Mc Cluskeys method:

$$F(A, B, C, D) = \Sigma m(1, 3, 4, 5, 9, 10, 11) + d(6, 8)$$

Unit-II

- 2. (a) Write the answer of following in one word:
 - (i) Which logic family has the highest fan in, fan out and lowest power dissipation?
 - (ii) Which logic family is the fastest among all logic families and what is its propogation delay time?
 - (b) Design CMOS NOR gate and NAND gate logicand write the advantages and disadvantages ofCMOS logic family.
 - (c) What is ECL logic? Why it is not so popular? Give advantages and disadvantage of it.

(d) Explain 2 i/p TTL circuit in detail. 7
Unit-III
3. (a) Drawa full adder circuit using two Half Adder circuit. 7
(b) Convert BCD to seven segment decoder. 7
(c) Design an even and odd parity bit generator using logic gates, if data is of 4 bits. 7
(d) (i) Implement the circuit for the given function using 4×1 MUX
F(A, B, C) = Σm(1, 3, 5, 6) 3½

(ii) Design 16: 1 MUX using 4: 1 MUX. 31/2

Unit-IV

- **4.** (a) Write excitation and characteristics table of JK flipflop.
 - (b) Construct a mod-5 synchronous binary up-down counter using T-flip-flop.
 - (c) Design a counter with the following sequence 0, 3,5, 6, and repeat.

2

(d) Implement: Less in resolution TVT on 1 malor (d)

	(i) 4 bit Ripple counter using D flip-flop.	31/2
	(ii) 4 bit ring counter.	3½
	Unit-V	
5.	(a) Explain the function of programmable Array logic.	2
	(b) Give the classification of semiconductor memory.	
	Explain them briefly why semiconductor memories are better than other.	7
	(c) Implement the following boolean function using PLA:	7
	$A(x, y, z) = \sum m(1, 2, 4, 6)$	
	$B(x, y, z) = \Sigma m(0, 1, 6, 7)$	
	$C(x, y, z) = \sum m(2, 6)^{2n}$,di
	$D(x, y, z) = \sum m(1, 3, 5, 7)$	
	(d) How to convert a Melay machine into Moore	
	man chine? Errolain with cuitable avanuale	- 7